REMARKS

Claims 1 and 3 through 10 are now pending in this application. In response to the non-final Office Action, dated February 24, 2005, claim 2 has been cancelled and claims 1, 3, 4, 6 and 9 have been amended. Care has been taken to avoid the addition of new matter. Favorable reconsideration of the application and allowance thereof are respectfully solicited.

Claims 1 through 4 and 6 through 8 have been rejected under 35 U. S. C. § 102(b) as being anticipated by U.S. patent 6,314,045 (Ikeda). Pages 2 and 3 of the Office Action set forth the rejection. Specific reference is made to the memory arrangement shown in Fig. 8. The connection gate circuit, recited in claim 1, has been read on connection control circuit 100 of Fig. 1.

Claims 5, 9 and 10 stand under objection for their dependency from a rejected claim. These dependent claims were indicated to be allowable if presented in appropriate independent form.

In response to the Office Action, claim 1 has been amended to include the recitation of claim 2, which has now been cancelled. Claims 3 and 4 have been amended to change their dependencies to claim 1. Claims 6 and 9 have each been rewritten in independent form to include the recitation of original claim 1. Withdrawal of the rejection and objection is believed appropriate.

Claim 1 now requires that the recited connection gate circuit comprise gates that are respectively activated by the sense amplifier activation signal and the column selection signal. It is submitted that the Ikeda column select gate IOG1 does not disclose such arrangement. The column select gate IOG1 of Fig. 8 of Ikeda is provided between a pair of bit lines and a pair of I/O lines to connect them together when activated. CE signals such as generated by the circuit of

Fig. 1 generates the activation signals for IOG1. The generation circuit of Fig. 1 is not connected between the bit lines and the I/O lines as stated in the Office Action.

Column select gate IOG1 and connection control circuit 100 of Ikeda do not form a circuit that meets the configuration of the connection gate circuit as defined in claim 1. The Office Action has read first and second gates of claim 2 (now claim 1) to correspond to Ikeda's Fig. 1 NAND circuit 101 and flip-flop 102, respectively, which, however, are not connected between a bit line pair and an I/O line pair in series. Moreover, Ikeda's Fig. 1 column bank address φCB is a signal activated when an operation reading/writing data from/to a bank is designated, rather than a column select signal for selecting a bit line pair. Flip-flop 102, considered in the Office Action to correspond to the second gate, does not conduct in response to the column select signal. Therefore, claim 1 and its dependent claims 3 through 5, are not anticipated by Ikeda.

Claim 3 additionally requires that the connection gate circuit further includes an equalize circuit equalizing potentials of a pair of nodes connecting the first gate with the second gate. It is submitted that the Office Action is in error in reading Ikeda's Fig. 8 bit line precharge/equalize circuit PE on the equalize circuit of claim 3. The equalize circuit of claim 3 is a circuit equalizing potentials of a pair of nodes connecting first and second gates included in the connection gate circuit, rather than equalizing a pair of bit lines, as in Ikeda.

Independent claim 6 requires, *inter alia*, a logic gate circuit activating that outputs a signal when the sense amplifier activation signal and the column selection signal are activated; and the connection gate circuit includes a gate that conducts in response to the output signal from the logic gate circuit. The Office Action has considered Ikeda's signal φCD to correspond to the claimed sense amplifier activation signal and Ikeda's signal CBi to correspond to the claimed

column select signal. However, Ikeda's signal φCD is activated when a read/write command is received and Ikeda's signal CBi is signal activated when an operation reading/writing from/to bank Bi is designated. Ikeda does not disclose a logic gate circuit activating an output signal when the sense amplifier activation signal and the column select signal are active. Therefore, claim 6 and its dependent claims 7 and 8, are not anticipated by Ikeda.

As claim 9 has been rewritten to include all the limitations of its previous parent claim, it is submitted that claims 9 and 10 are now allowable.

Withdrawal of the rejection and objection, and allowance of the application, are respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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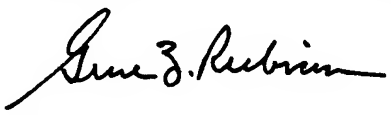

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